A STUDY OF Si/SiGe n-MOSFET PROCESSED AND UNPROCESSED CHANNEL LAYERS USING FIB AND TEM METHODS

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Introduction
The 4.2% lattice mismatch between Si and Ge atoms can be employed to create high mobility strain-engineered devices [1]. In addition to Si substrates, upon which SiGe can be grown under compressive strain pseudomorphically, a compositionally graded SiGe virtual substrate (VS) can be grown as a thick graded buffer layer [2]. This layer enables complete relaxation of lattice mismatch strain via purposeful misfit dislocation generation, which is contained within the VS. This allows Si to be grown on tensile strain onto a dislocation free constant composition SiGe layer, thus creating a high mobility $n$-channel [3]. In this study, we look at state of the art Si/SiGe dual $n$-channel MOSFET devices as well as their corresponding unprocessed blanket layers grown on such graded VS with a constant composition SiGe buffer layer. Dual channel architectures increases the robustness of the material to strain relaxation by the sequential growth of tensile and compressively strained layers, while band offsets between the oppositely strained materials can be used to create high mobility surface $n$-and buried $p$-channel MOSFETs. Here, stress-relief layers are grown into the VS on the processed layers to aid threading dislocation confinement. Wafer centre and edge layers are also compared to reveal any growth discrepancies (ie. Ge conc. and channel layer thickness). Focused ion beam (FIB) cross-sectioning methods [4] have been adopted to prepare site specific TEM samples of sub-micron gate length devices to compare with the conventional mechanically polished and Ar⁺ ion milled unprocessed blanket layers.

Fig 1: (a) Low mag. STEM BF micrograph of centre wafer processed device layer illustrating VS with stress-relief layers confining threading dislocations and MOSFET gate perched above. (b) Ge conc. profile measured along VS detailing a ~15 atomic % peak as intended. (c) High mag. STEM BF micrograph of gate structure. (d) High mag. STEM HAADF micrograph under gate structure, showing diffused Si$_{0.85}$Ge$_{0.15}$ (~15 nm) strained layer, Si cap (~8 nm) and SiO$_2$ layer.

Fig 2: Wafer edge processed device: (a) Low mag. STEM BF micrograph of device sitting on VS layer structure. (b) Ge conc. profile along VS detailing a ~8 atomic % peak, lower than the intended 15 %. (c) High mag. STEM BF micrograph under gate structure, showing diffused Si$_{0.85}$Ge$_{0.15}$ (~8 nm) strained layer, Si cap (~4 nm) and SiO$_2$ layer.

Fig 3: Wafer centre blanket layer: (a) STEM BF micrograph of VS and buffer layer, showing contained threading dislocations. (b) Ge conc. along VS detailing a peak of ~15 atomic % , as intended. (c) High mag. STEM HAADF micrograph of channel layers, showing an abrupt Si$_{0.85}$Ge$_{0.15}$ strained layer (~11 nm) and Si cap (~14 nm).

Fig 4: Wafer edge blanket layer: (a) Low mag. STEM BF micrograph of VS and buffer layer. (b) Ge conc. profile along VS detailing a ~15 atomic % peak. (c) High mag. STEM BF micrograph of abrupt channel layers: a ~11 nm Si$_{0.85}$Ge$_{0.15}$ strained layer and ~7 nm Si cap.

Conclusions
● TEM results have shown that whilst unprocessed blanket layers have abrupt channel layer interfaces which display general accordance with the desired growth parameters; the channel layers under the gate stack in processed $n$-MOSFET devices all exhibit diffused interfaces.
● High thermal budgets (~800 °C) normally practiced in gate oxidation and annealing may be the cause of such interface diffusion which would lead to degradation of carrier mobility.
● Reported differences in the Si channel layer thicknesses between the wafer centre and edge may be attributed to radial variations in growth rates [5] grown by ULPVD in a modified MBE reactor.

References